Code.No: **RR 311901** | **RR** | **SET-1**

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
DIGITAL SYSTEM DESIGN
(ELECTRONICS AND COMPUTER ENGINEERING)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

- - -

1.a) Explain briefly the cube based operations.
b) Apply C_{AMP} algorithm and minimize the following Boolean function.
f(A,B,C,D) = Σ (2 ,3 ,4, 5,6,7, 8,10,11,12,13,15). [8+8]

2.a) Define the following terms.
i) Essential prime cube ii) Valid selective prime cube
b) Determine if the cubes 2221 and 1212 are wholly with in the function.
f = 0112+1002+221+2112. [8+8]

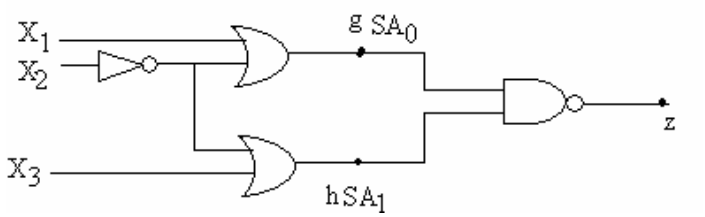
3. Design a digital system which performs a full subtraction on two register data (RA and RB) having unsigned binary number. Store result in RA register. Draw an ASM chart to control the operation of this subtractor. Realize the input using D flip flops and MUX'S. [16]

4.a) Tabulate the PAL programming table for the given combinational circuit's truth table.

INPUT			OUTPUT			
X	Y	Z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

b) What are the advantages and disadvantages of PLD'S. [8+8]

5. Apply path sensitization technique to detect the mensional faults as shown below. Verify the same using Boolean difference method for the same. [16]



6. Design a test pattern generation to test the following sequential unit.

PS	NS , 2	
	X = 0	X = 1
A	B,1	A,1
B	E,1	A,1
C	A,0	E,1
D	C,1	D,1
E	E,0	D,1

[16]

7. Explain compact algorithm for the PLA

COL	SSRS
A	4,5,10
B	1,2,3,6,11,12
C	2,9
D	4,7,8,9,10
E	3,5,6,10,11
F	1,5,7,8,12
G	1,2,3,7,9,12
H	3,9

[16]

8. Write a brief note on:
   a) Fault model in PLA
   b) DFT schemes. [8+8]

--ooOoo—

Code.No: **RR 311901** | **RR** | **SET-2**

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
DIGITAL SYSTEM DESIGN
(ELECTRONICS AND COMPUTER ENGINEERING)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

\- - -

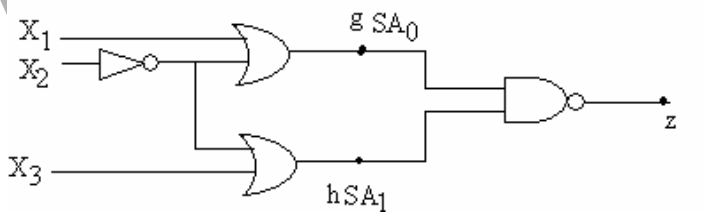
1. Design a digital system which performs a full subtraction on two register data (RA and RB) having unsigned binary number. Store result in RA register. Draw an ASM chart to control the operation of this subtractor. Realize the input using D flip flops and MUX'S. [16]

2.a) Tabulate the PAL programming table for the given combinational circuit's truth table.

INPUT			OUTPUT			
X	Y	Z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

b) What are the advantages and disadvantages of PLD'S. [8+8]

3. Apply path sensitization technique to detect the mensional faults as shown below. Verify the same using Boolean difference method for the same. [16]



4. Design a test pattern generation to test the following sequential unit.

PS	NS , 2	
	X = 0	X = 1
A	B,1	A,1
B	E,1	A,1
C	A,0	E,1
D	C,1	D,1
E	E,0	D,1

[16]

5. Explain compact algorithm for the PLA

COL	SSRS
A	4,5,10
B	1,2,3,6,11,12
C	2,9
D	4,7,8,9,10
E	3,5,6,10,11
F	1,5,7,8,12
G	1,2,3,7,9,12
H	3,9

[16]

6. Write a brief note on:
   a) Fault model in PLA
   b) DFT schemes. [8+8]

7.a) Explain briefly the cube based operations.
   b) Apply C_{AMP} algorithm and minimize the following Boolean function.
   f(A,B,C,D) = Σ (2 ,3 ,4, 5,6,7, 8,10,11,12,13,15). [8+8]

8.a) Define the following terms.
   i) Essential prime cube ii) Valid selective prime cube
   b) Determine if the cubes 2221 and 1212 are wholly with in the function.
   f = 0112+1002+221+2112. [8+8]

--ooOoo--

Code.No: **RR 311901** | **RR** | **SET-3**

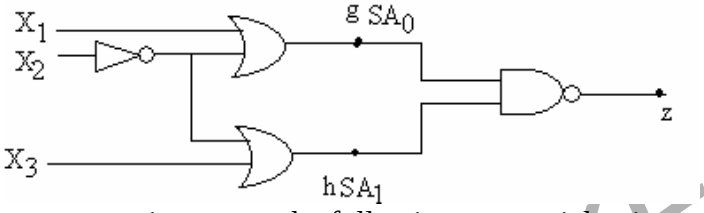
III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
DIGITAL SYSTEM DESIGN
(ELECTRONICS AND COMPUTER ENGINEERING)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

- - -

1. Apply path sensitization technique to detect the mensional faults as shown below. Verify the same using Boolean difference method for the same. [16]



2. Design a test pattern generation to test the following sequential unit.

PS	NS , 2	
	X = 0	X = 1
A	B,1	A,1
B	E,1	A,1
C	A,0	E,1
D	C,1	D,1
E	E,0	D,1

[16]

3. Explain compact algorithm for the PLA

COL	SSRS
A	4,5,10
B	1,2,3,6,11,12
C	2,9
D	4,7,8,9,10
E	3,5,6,10,11
F	1,5,7,8,12
G	1,2,3,7,9,12
H	3,9

[16]

4. Write a brief note on:
   a) Fault model in PLA
   b) DFT schemes. [8+8]

5.a) Explain briefly the cube based operations.
   b) Apply C_{AMP} algorithm and minimize the following Boolean function.
   f(A,B,C,D) = Σ (2 ,3 ,4, 5,6,7, 8,10,11,12,13,15). [8+8]

6.a) Define the following terms.
i) Essential prime cube ii) Valid selective prime cube

b) Determine if the cubes 2221 and 1212 are wholly with in the function.
f = 0112+1002+221+2112. [8+8]

7. Design a digital system which performs a full subtraction on two register data (RA and RB) having unsigned binary number. Store result in RA register. Draw an ASM chart to control the operation of this subtractor. Realize the input using D flip flops and MUX'S. [16]

8.a) Tabulate the PAL programming table for the given combinational circuit's truth table.

INPUT			OUTPUT			
X	Y	Z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

b) What are the advantages and disadvantages of PLD'S. [8+8]

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Code.No: **RR 311901** | RR | SET-4

III B.TECH – I SEM EXAMINATIONS, NOVEMBER - 2010
DIGITAL SYSTEM DESIGN
(ELECTRONICS AND COMPUTER ENGINEERING)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

- - -

1. Explain compact algorithm for the PLA

COL	SSRS
A	4,5,10
B	1,2,3,6,11,12
C	2,9
D	4,7,8,9,10
E	3,5,6,10,11
F	1,5,7,8,12
G	1,2,3,7,9,12
H	3,9

[16]

2. Write a brief note on:
   a) Fault model in PLA
   b) DFT schemes. [8+8]

3.a) Explain briefly the cube based operations.
   b) Apply C_{AMP} algorithm and minimize the following Boolean function.
   f(A,B,C,D) = Σ (2 ,3 ,4, 5,6,7, 8,10,11,12,13,15). [8+8]

4.a) Define the following terms.
   i) Essential prime cube ii) Valid selective prime cube
   b) Determine if the cubes 2221 and 1212 are wholly with in the function.
   f = 0112+1002+221+2112. [8+8]

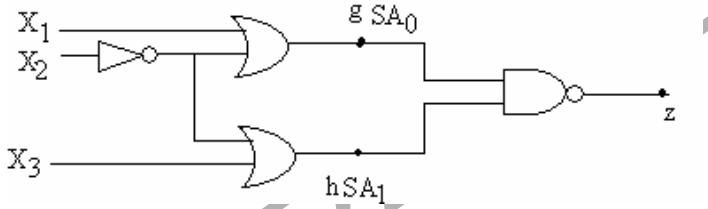
5. Design a digital system which performs a full subtraction on two register data (RA and RB) having unsigned binary number. Store result in RA register. Draw an ASM chart to control the operation of this subtractor. Realize the input using D flip flops and MUX'S. [16]

6.a) Tabulate the PAL programming table for the given combinational circuit's truth table.

INPUT			OUTPUT			
X	Y	Z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	0	1	0
1	0	1	0	0	0	1
1	1	0	1	1	1	0
1	1	1	0	1	1	1

b) What are the advantages and disadvantages of PLD'S. [8+8]

7. Apply path sensitization technique to detect the mensional faults as shown below. Verify the same using Boolean difference method for the same. [16]



8. Design a test pattern generation to test the following sequential unit.

PS	NS , 2	
	X = 0	X = 1
A	B,1	A,1
B	E,1	A,1
C	A,0	E,1
D	C,1	D,1
E	E,0	D,1

[16]

--ooOoo--